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Novel Topology for Four-Quadrant Converter

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Abstract

Particle accelerators, like the LHC (Large Hadron Collider), make use of true bipolar power converters to feed superconducting magnets. Moreover, the LHC imposes that most converters must be installed underground. This constraint leads to the necessity of a high efficiency and a reduced volume for all the power converters. In this paper, the authors present a novel four-quadrant topology composed by an association of a ZVS-inverter and a ZCS-rectifier. This DC-AC-DC converter is fully reversible and a soft-switching operation mode is achieved for all switches over the full operating range. After a thorough analysis of the prototype design [±600A, ±10V], simulation and experimental results confirm the general performance of this power structure.

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1. Introduction

The European Laboratory for Particle Physics (CERN) is a European intergovernmental organisation with 19 Member States. It has its seat in Geneva but straddles the Swiss-French border. Its objective is to provide for collaboration among European States in the field of high energy particle physics research and to this end it designs, constructs and runs the necessary particle accelerators and the associated experimental areas. At present more than 5000 physicists from research institutes world-wide use the CERN installations for their experiments. The Large Hadron Collider (LHC) is the next approved accelerator being constructed on the CERN site [1]. The LHC machine will mainly accelerate and collide 7 TeV proton beams but also heavier ions (up to lead). It will be installed in the existing 27 km circumference tunnel, about 100 m underground, presently housing the Large Electron Positron collider (LEP). The LHC design is based on superconducting twin-aperture magnets which operate in a superfluid helium bath at 1.9 K. This machine is scheduled to come into operation in the year 2005.
The superconducting LHC accelerator requires high currents (13kA) and relatively low voltage (~10V) for its main magnets and makes extensive use of true bipolar power converters [±600A, ±10V] to correct the multipole errors of the main superconducting magnets [2]. These power converters will feed sextupole and decapole spool piece circuits as well as octupole magnets. Several trim magnets also require 600A four-quadrant converters. In total there will be around 500 converters [±600A, ±10V]. Moreover, about 720 converters [±60A,±8V] (for the arcs) and about 260 converters [±120A,±8V] (in the 8 straight regions) will enable correction of the closed orbit of the beams.
The high number of converters and the necessity that all of the above four-quadrant power supplies must be installed underground, impose a volume optimisation and a high performance (DC stability, dynamic response, efficiency, EMC,…) for all converters.
The main requirements can be summarised as follows:

- High precision (< 50 ppm).
- Galvanic isolation between main network and superconducting magnets or loads.
- Water cooling of the converters is mandatory.
- Reparability. All power converters must be designed with fast plug-in modules and the weight of each one must not exceed 25 kg to allow a fast exchange.
- Very high reliability and operational redundancy.

Presently, the two normal industrial ways to provide a four-quadrant topology are : 1) the double converters (anti-parallel thyristor bridges with circulating current) and 2) the association of a 50 Hz transformer to assure the galvanic isolation,a diode rectifier and a PWM inverter. Both methods present some disadvantages, particularly the volume and weight of 50 Hz transformers, inductors and passive filters. In addition, the presence of two conversion stages, working at low voltage and high current, leads to low efficiency, and the hard switching inverter operation with high current introduces important EMI problems.
To improve the performance of the above structure, a unipolar soft-switching converter can replace the first conversion stage (Fig. 1). The output PWM inverter works mainly as a polarity switch and commutates (or becomes linear) only at a low voltage. The efficiency and volume are improved, but in any case, the structure is not fully reversible and an additional resistance (brake chopper) must be included to dissipate the energy when the superconducting magnet is acting as a generator.

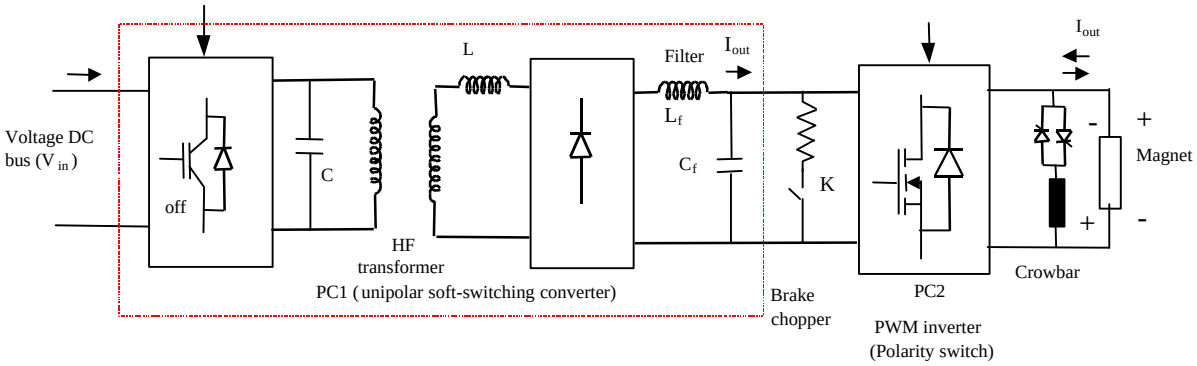


Fig. 1: Improved topology for a four-quadrant converter

A prototype was developed at CERN where the first conversion stage is a quasi-resonant converter working at 35 kHz and the output inverter switches at 100 kHz when the output voltage is lower than half a volt [3]. Moreover, two present contracts are based on this topology where the input and output converters were replaced by a soft-switching inverter working at 30 kHz (PC1 is a ZVZCS PWM inverter [5]) or 50 kHz (PC1 is a ZVS resonant converter [6]) and by a Mosfet polarity switch which handles the magnet energy dissipation. The main drawback of these topologies is that the magnet energy must be dissipated at the level of the output stage (low voltage). An other disadvantage is the limited operation area of the input converter. Because of the diode rectifier, operation is limited to quadrant 1, which requires the output converter for operation in quadrant 3 and a brake chopper to operate in quadrants 2 and 4. Moreover, soft-switching operation of input converter is only achieved for current above a threshold (function of input voltage and passive elements) so that the brake chopper is necessary in some regions of quadrant 1.

The present work was launched to study a soft-commutated fully reversible topology and to compare this topology with the previous ones.

The paper introduces a controlled turn-on rectifier instead of the diode rectifier. This new topology, presented in Fig. 2, realises a direct DC-DC fully reversible energy conversion where, unlike a classical structure, all semiconductors have a soft-switching operation mode.

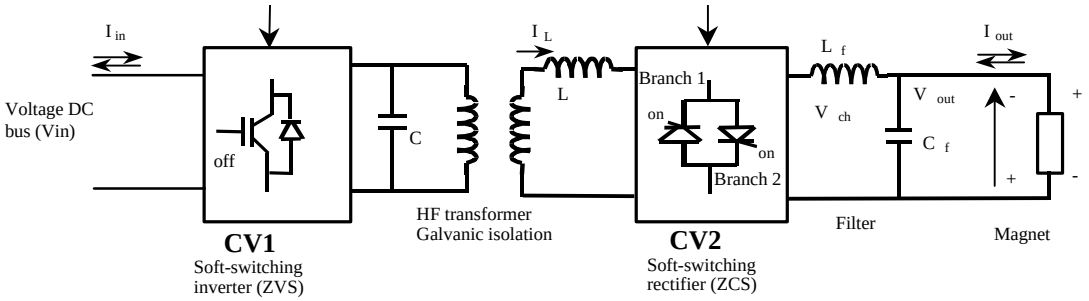


Fig. 2: New four-quadrant soft-switching converter

2. New four-quadrant topology

The block diagram is composed of an inverter (CV1), a HF step-down transformer and ZCS-rectifier (CV2; composed of two branches BR1 and BR2). This association of dual-converters is connected to an input DC voltage source and to an output current source (magnet). The topology is direct: connection from input source to output source uses only semiconductors. Without any reactive elements, the input inverter must be a hard-switched voltage –source inverter; nevertheless, a series inductor inside the AC link (the leakage inductance of transformer) allows delaying the current with respect to voltage

waveforms and gives the conditions of spontaneous turn-on. Like this, the input inverter is only turn-off controlled and based on dual-thyristors. In short, the ZVS-inverter produces an AC voltage which ensures the soft switching conditions of ZCS-inverter. This ZCS-inverter imposes an AC current on ZVS-inverter output to allow the natural switching of dual-thyristors.

In some regions $\left(I_{out}\sqrt{L/C} \geq V_{in}\right)$, the output converter CV2 can be controlled to operate as a diode rectifier and the same operation as with the unipolar above described topology is achieved. This operation is very efficient, because the current in the AC link never exceeds the output DC current (mode 1). When antiparallel thyristors are used in the rectifier CV2, the conditions of operation are the dual of those of inverter CV1. The capacitor gives the conditions of soft turn-off for CV1 and the inductor provides soft turn-on for CV2.

The number of degrees of freedom is increased by the use of controlled switches on the secondary side and the phase-shifts between the primary and the secondary side switches are controlled. The magnitude and the polarity of the load current are controlled at constant switching frequency and soft commutation can be obtained for any value of the input voltage and output current.

Like in the one-quadrant topology, the phase-shift between the two legs of the inverter can be used to ensure the continuity of the operation in the four quadrant.

The continuity of the operation in the four quadrants and the corresponding control pattern will be detailed below.

2.1. State-plane-analysis

Three parameters can be used to control the converter:

γ : phase-shift between the two legs of the inverter

θr : phase-shift between the primary-side switches and the secondary-side switches BR2 (Fig. 2)

θr' : phase-shift between the primary-side switches and the secondary-side switches BR1

Depending on these 3 phase-shifts and the value of the normalised load current, three main different modes of operation are possible and the corresponding state planes are represented in Fig. 3.

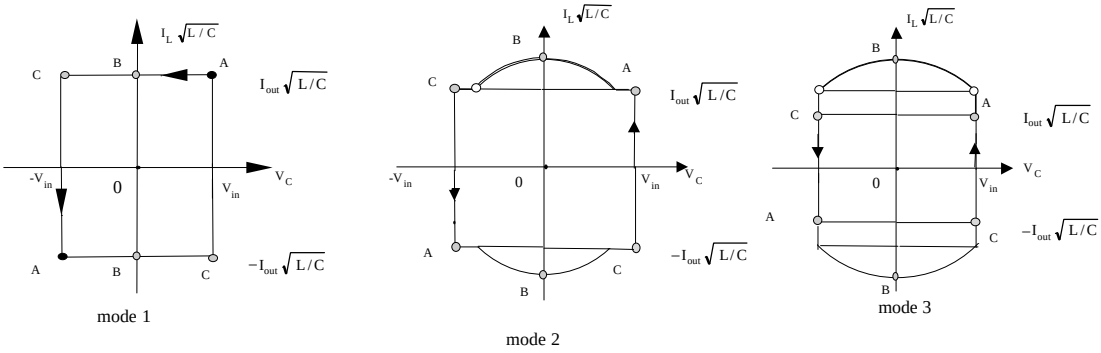


Fig. 3: State planes of the different modes of operation

In mode 1, only one branch of CV2 is used (BR1 if the load current is positive and BR2 when the load current is negative). This mode is possible only for high current and no over current is necessary to achieve ZVS and ZCS.

If the current is positive, θr is not used as the bridge BR2 is never conducting, but γ is used to control the power flow. This parameter controls the duration of the fixed active points A and C on the state plane, so that the load average voltage can be positive or negative. The parameter γ can be also used in addition to θr'. This additional phase-shift introduces a freewheeling stage in the circuit, which is marked by the fixed point B on the state plane. When the current is negative, the bridge BR2 is only used in mode 1 and symmetrically θr and γ can be used to control the magnitude and the polarity of the load current. In mode 2 and 3, the operation is the same as in mode 1, but the 2 parameters θr and θr' are used simultaneously: a) with positive current, θr will be controlled to obtain soft commutation at

low current (even at zero current), while θr' acts as in mode 1; b) with negative current, θr' will be symmetrically used to achieve ZVS and ZCS, while θr is used as in mode 1.
The soft commutation control parameters can be defined to obtain an optimal peak current in the AC link. The duration of each sequence, the steady conversion ratio and the expressions of the current and voltage stresses of the different components are derived using the state plane. The resonant elements can be designed for minimum stresses according to the converter specifications.

2.2. Control strategies

These converters offer many degrees of freedom, hence the same point of operation can be obtained with different control patterns. These degrees of freedom are used to control the output voltage and the resonant current. Regarding the control strategy, a reasonable approximation is to neglect the commutation phenomena and to assume the waveforms are square waveforms. There are two ways to control the output voltage (Fig. 4.1).

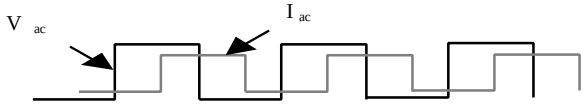


Fig. 4.1a : two-level voltage waveform

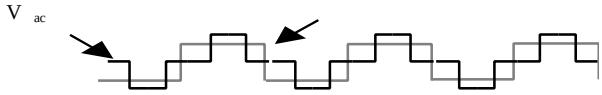


Fig.4.1b : three-level voltage waveform

Fig. 4.1: Output voltage control

With γ=0 (Fig. 4.1a), the voltage and current waveforms in the AC link (transformer) are two-level square waveforms with 50% duty cycle, and the output voltage is set by adjusting the phase shift between the voltage and current waveforms. Varying this voltage between 0 and 180° allows varying the output voltage from the minimum (negative) value to the maximum (positive) value in a smooth way. The voltage zero-crossing corresponds to 90° phase-shift and requires no special attention.
However, it should be noted that depending on the sign of the current, this phase shift is controlled by either θr' (positive current), or θr (negative current), which means that the current zero-crossing is a particular point and requires thorough analysis. As a conclusion, this mode of operation allows operation in the 4 quadrants, but a discontinuity in the control pattern might appear at zero current (Fig. 4.2). The exact characteristics between current (x), voltage (q) and control angles (θr'and θr), are given in Fig. 4.3.
A second type of control involves using γ to generate a three-level waveform in the AC link (Fig. 4.1b). The variation of the output voltage can then be totally achieved by the primary converter, which leaves θr' and θr for other purposes. The exact value for γ to obtain a given output voltage for different currents is given in the plot of Fig.4.4.
The former remarks give a general understanding of the operation of this converter, but the soft commutation operation requires special conditions at the switching time. The general idea is that a resonant network composed of the snubber capacitors of the ZVS inverter and the leakage inductance of the transformer, will provide the current pulses required to obtain ZVS and ZCS conditions. To optimise the overall operation, the control pattern must be chosen to reduce these current pulses to the minimum value compatible with soft switching. To achieve smooth zero-crossing of the current, it seems preferable to use another mode of operation in which half of the thyristors are continuously fired and behave as diodes. This mode allows reaching the four quadrants but it is then the voltage zero-crossing that introduces a discontinuity (Fig.4.5). In that case, the phase-shift is imposed by the diodes, and the current overshoots are controlled with the firing angles of the thyristors (θr = θro for q>0; for q<0; θr'= θro'; see Fig. 4.6). Finally, to allow safe zero-voltage or zero-current transition, the combination of modes B and C was chosen, as is illustrated in Fig. 4.7.

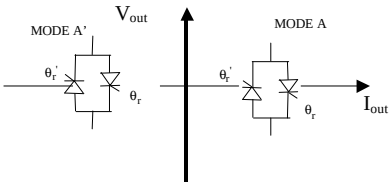


Fig.4.2: Voltage reversible topologies

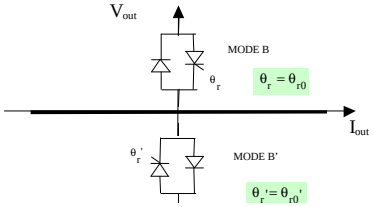


Fig. 4.5 Current reversible topologies

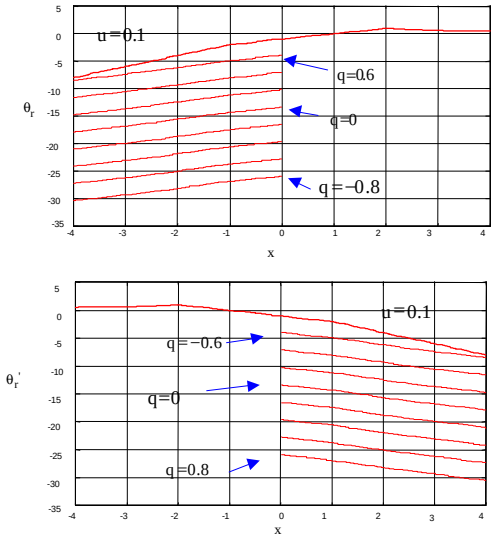


Fig. 4.3: Steady characteristics of the first method with $\gamma = 0$

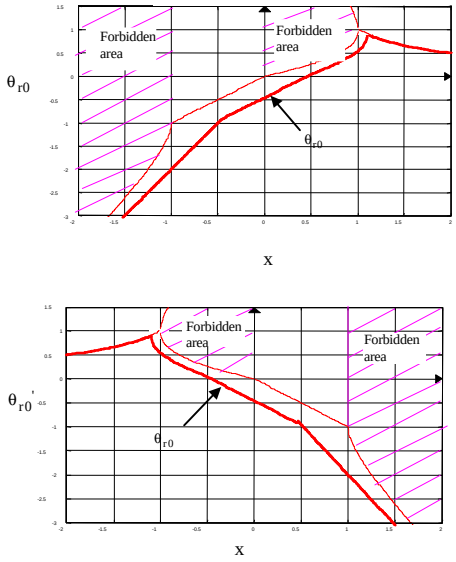


Fig.4.6: Control characteristics of current reversible topologies

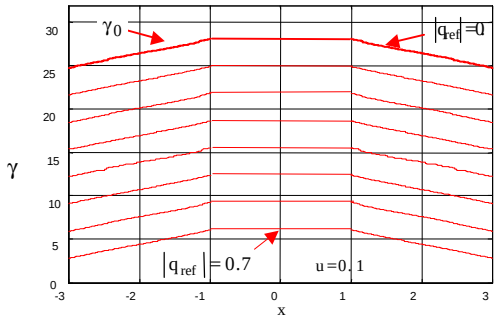


Fig. 4.4: Characteristics of γ

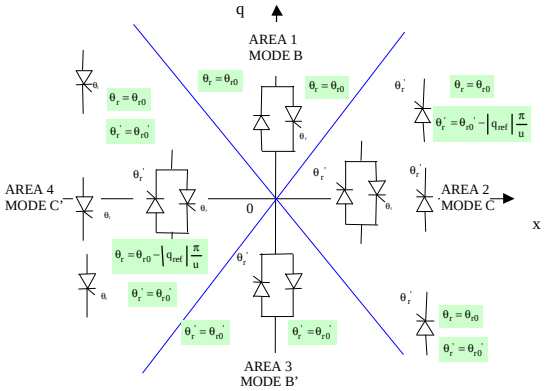


Fig. 4.7: Combination of the different topologies

2.3. Simulation results

To verify the analysis, the simulation of a [±600A,±12V] LHC power converter has been done.

The specifications of the converter are as follows:

Vin = 540 V

-12 V < Vout < +12 V

L = 40µH ; C = 2.3 nF ; f = 50 kHz

-7.2 kW < P < 7.2 kW

-600 A < Iout< 600 A.

Transformer turn ratio: 1:34

Figures 5 shows the results, for the 2 methods of control.

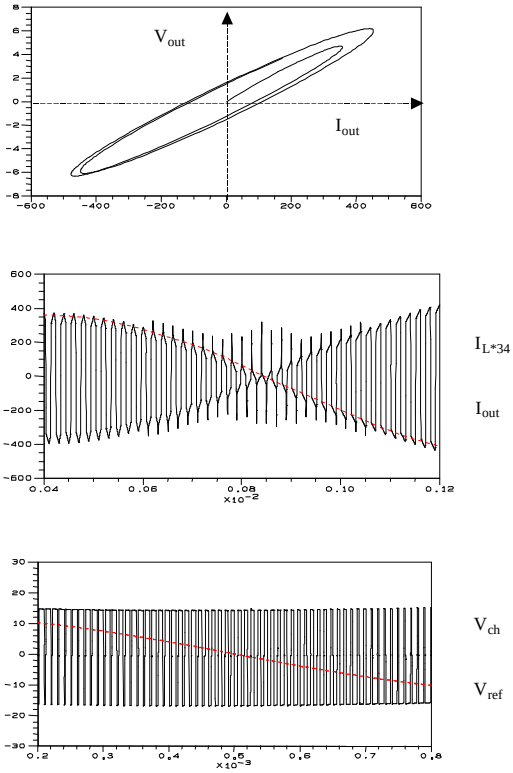


Fig.5.1: First method of operation with γ =0

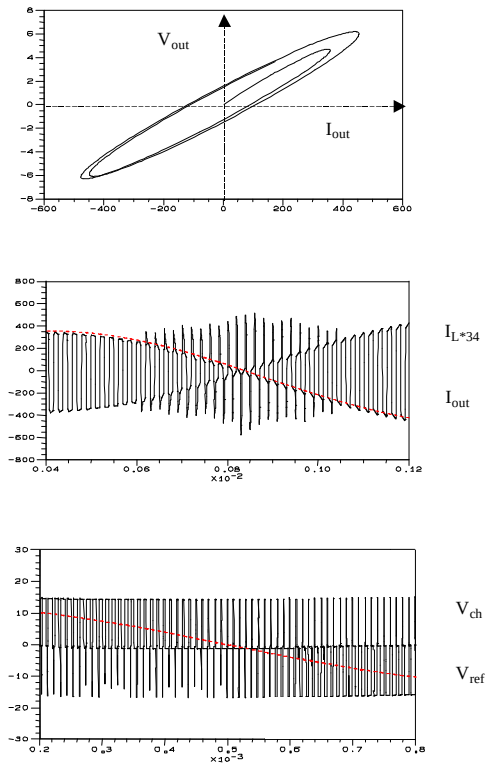


Fig.5.2: Second method of operation using γ

Fig. 5 Simulation results

3. DC-AC-DC prototype

3.1. [±600A,±12V] power unit

According to the LHC specifications, a [±600A,±12V] prototype circuit has been built (Fig. 8). The design principle is shown in Fig. 6.

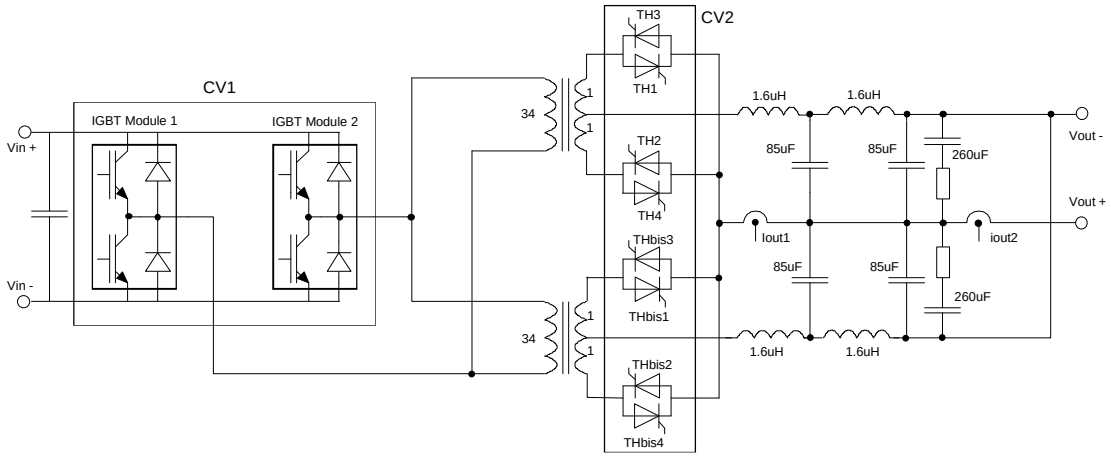


Fig 6: Prototype [±600A,±12V]: Power Part Diagram

The Insulated Gate Bipolar Transistors (IGBTs) are used at the primary-side as dual thyristors. The dual thyristor control logic drivers are integrated inside the APT® power modules. The parasitic capacitors of 1 nF for each IGBT are sufficient to obtain the soft-commutation conditions. No snubber capacitors are then necessary.
The power converter uses a high frequency transformer of 7.2 kW with a transformer ratio of 34 and a low leakage inductance around 25µH. This is achieved by using with two step-down transformers with classical ferrite coils in parallel. This solution reduces the leakage inductance by a factor of 2 compared with a single transformer. The leakage inductance of each transformer is equal to 20µH. Finally, the total inductance measured from the primary side with the two transformers, the busbars and the controlled rectifier is 25µH at 100kHz

The controlled rectifier CV2 is made with one rectifier on each secondary-side of the transformers. It is realised with Power Mosfet and Schottky diode devices. All the components are mounted on 5 water-cooled metal sheets, to dissipate the commutation and conduction losses at 50kHz. The assembly is very compact to reduce the leakage inductance. An equivalent high-frequency thyristor is realised with 2 parallel Power Mosfets and 2 parallel Schottky diodes and these components are placed in series (Fig. 7). The Power Mosfets are driven with a thyristor control logic which is achieved by measuring the voltage across the diodes. When the diodes are ON the voltage is ~0.3V. The driver detects when the diode voltage exceeds -1V (diode turns OFF) and blocks the Mosfet after 600ns (recovery time modelling tq). The thyristor turn-on time is close to 300ns.

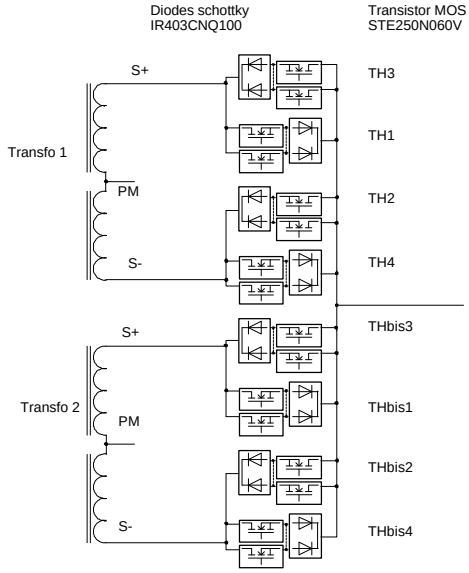


Fig 7 : ZCS output converter layout

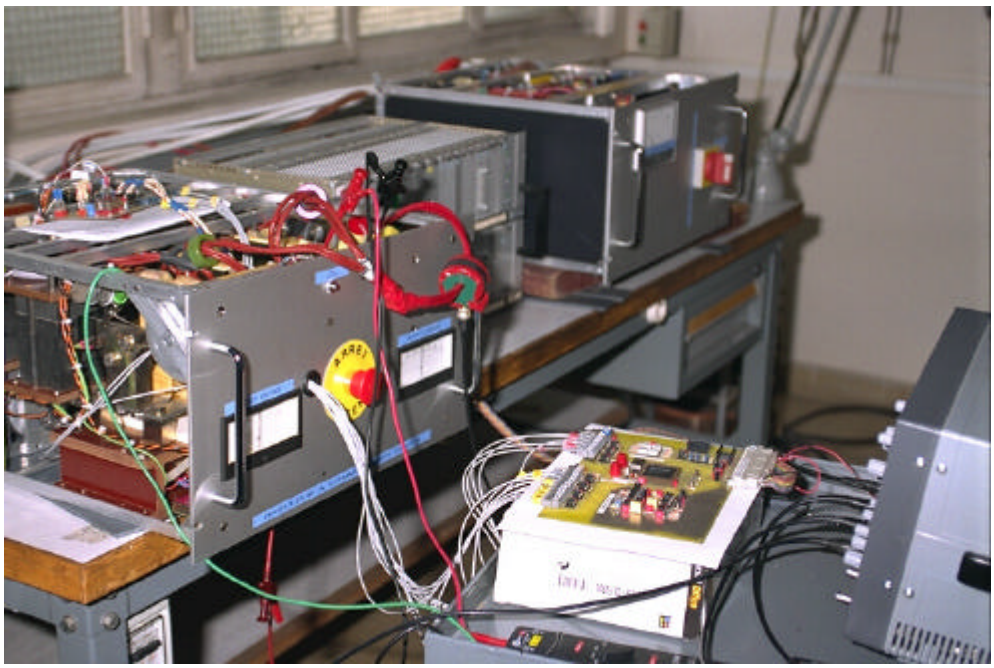


Fig. 8: [±600A,±12V] Prototype Photo

3.2. Control unit

At high switching frequencies, the problem of processing suitable digital algorithms in real-time becomes one of the predominant problems to be solved. Several semiconductor manufacturers offer analogue control chips, which meet the timing constraints. These chips implement simple but fast primitives (comparators, PWM blocks, etc.) and are designed to cover standard control algorithms. Configuration is done by the user via external interconnections.
With regard to the present DC-DC reversible converter, the complex control algorithm suggests an all-digital control approach based on a Field-Programmable Gate Array (FPGA). The parallel computing capability of these devices places FPGAs in an ideal position to serve as a hardware platform, not only for rapid prototyping, but for series production.

The unit control uses a single XILINX XC4010E FPGA device. The principal system tasks are summarised as follows:

- The start-up of the DC-DC converter is assured by a hard turn-on control applied simultaneously to the dual-thyristors (TD1 and TD4) and thyristor TH1.
- The delay angles of thyristors (θr, θ'r and γ) and the operation mode are determined as a function of output current and reference output voltage.

The simplified control algorithm is shown on Fig. 9. The core of the proposed controller consists of several additions and multiplications, which implement the control algorithm. For example, for a positive current, the control pattern is continuously defined by the operations shown in Fig 10.

XC4000E FPGA devices can run at synchronous system clock rates of up to 66MHz and internal performance can exceed 150MHz. With a 12MHz clock, an edge resolution of 40ns is achieved. This system clock determines a resolution of 8 bits for control parameters and a converter switching frequency of $f_s \approx 50$ kHz. In conclusion, depending on the output current and DC voltage reference, the prototype card generates the switch control pulses, which feed optic fiber IGBT drivers at a constant frequency.
To achieve a higher current and voltage resolution, it is necessary to use a large amount of FPGA area to implement mathematical operations. When implementing multipliers, generally a fully parallel-array alternative is used. In this parallel approach, the multiplication rate is just the delay through the combinatorial logic. Nevertheless, the physical area constraint demands more than one FPGA device. Part of future development involves investigating mixed EEPROM/FPGA solutions. This architecture is an attractive approach to implement the above-described solutions and to improve converter features.

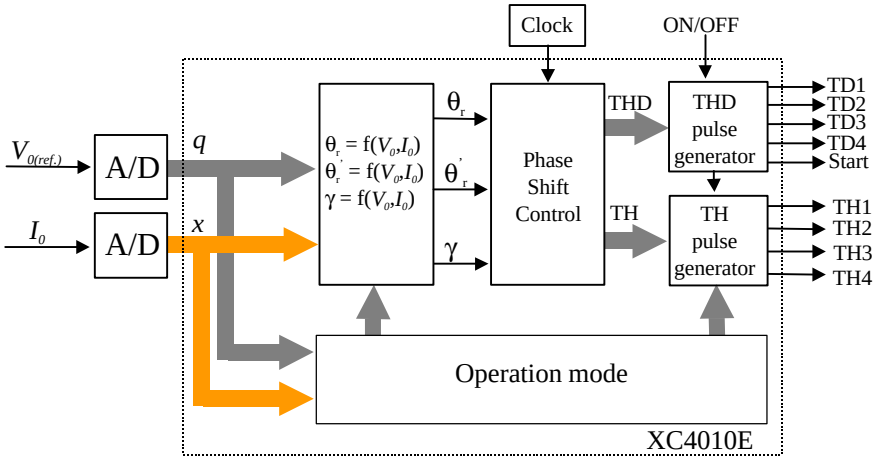


Fig. 9: Schematic block of control card

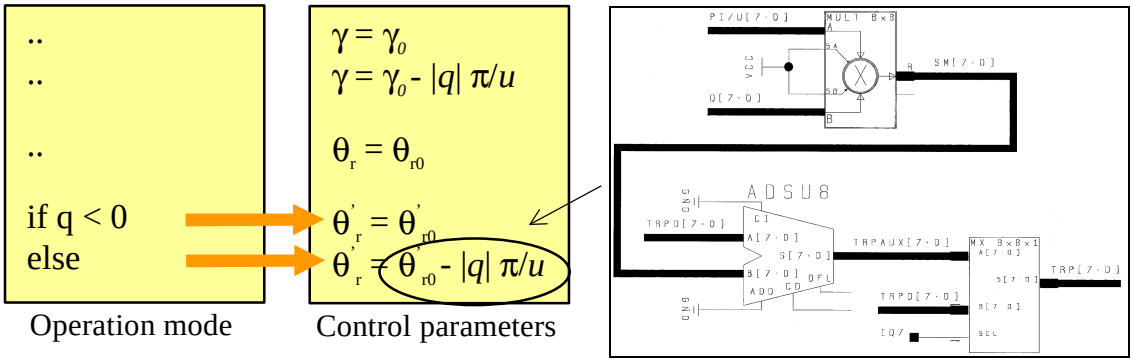
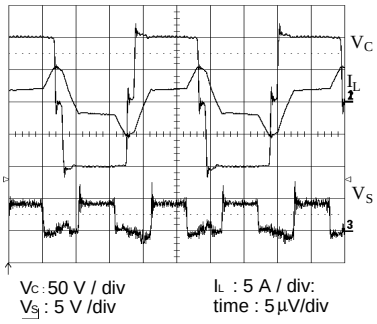


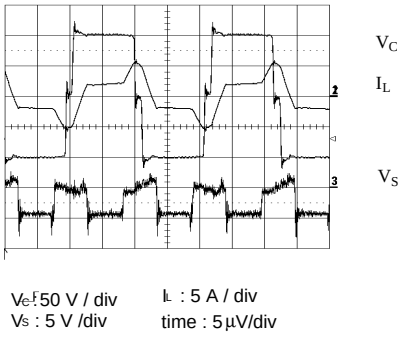
Fig. 10: Schematic block of control card

3.3. Experimental results

The Figure 11 and 12 presents the first experimental results at low input voltage (Vin = 100V) for the two methods of control (with and without phase-shift between the two-legs of the inverter). These results show the four-quadrant behaviour and prove that the soft-commutation conditions are fulfilled for all the operation modes and especially at low and zero output current. A thorough evaluation of the prototype is under progress and particularly a comparison of various control strategies at full power.



MODE 3 (Positive output voltage)



MODE 3' (Negative output voltage)

Fig. 11 : Experimental results (method using γ)

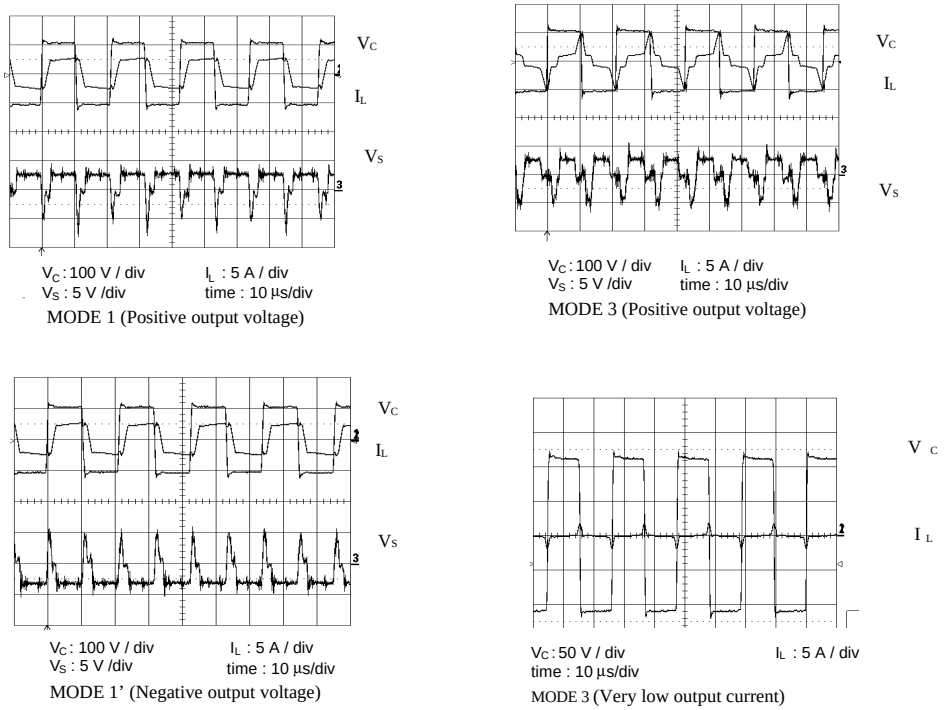


Fig. 12: Experimental results (with $\gamma = 0$)

4. Conclusion

The main advantages of the novel four-quadrant topology, presented in this paper, are the suppression of the high current output PWM inverter and the output brake chopper. Furthermore, soft-commutation is achieved in all the switches over the full range of operation. According to the application, the first converter (AC/DC converter) could be a three-phase six-pulse diode rectifier (energy dissipation at high voltage at the level of the DC bus) or a classical PWM converter (energy regenerated to the mains). A [±600A,±12V] prototype has been built and the first results confirm the analysis of all the operational modes. Several control strategies are under evaluation to optimise the quadrant changes (zero current and zero voltage crossings).

REFERENCES

1. http://www.cern.ch and http://wwwlhc01.cern.ch/lhcpub/Welcome.html
2. F. Bordry, A.Dupaquier, *"High Current, Low Voltage Power Converters for LHC. Present Development Directions "*, European Particle Accelerator Conference, EPAC'96, Sitges, June 1996
3. J. Benavent, F. Bordry, J. Carrasco, E. Dede, A. Dupaquier, *"On the design of a high power four quadrant power converter for superconducting magnets"*, EPE'97, Trondheim (Norway), Sept 97
4. F. Bordry, P. Coulibaly, A. Dupaquier, T. Meynard, *"Novel Topology [±600A,±12V] four quadrant converter"*, Electrical Power Technology in European Physics Research (EP2) , Grenoble, France, Oct 98.
5. F. Bordry, A. Dupaquier, G. Kniegl, R. Weber, *"Four-Quadrant Converter [±600A,±12V]. Prototype for LHC"*, Particle Accelerator Conference PAC99, New-York, Mars 99
6. F. Bordry, P. Cussac, A. Dupaquier, *"High Precision and High Frequency Four-Quadrant Power Converter [±600A,±12V] "*, 8th European Conference on Power Electronics EPE'99, Lausanne, Sept 99
7. P. Coulibaly, "Convertisseurs réversibles à commutation douce", Thèse de doctorat, Institut National Polytechnique de Toulouse, Décembre 98